JIACHENG PAN

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Summary

Jiacheng Pan is a Staff ASIC Design Engineer in Enflame Tech in Shanghai, with a focus on architecture exploration and modeling, and hardware-software co-design for domain-specific accelerators for deep learning applications. He was a GPU SM architect in NVIDIA, software engineer in AMD and RnD engineer in Synopsys.

His research interest includes computer architecture design, hardware-software co-design, high performance computing, EDA algorithms, and ASIC design.

Education

September 2009 - June 2013 | **Fudan University, Shanghai**
Bachelor of Science in *Microelectronics*
Secondary Major in *Economics*

January 2017 - May 2019 | **Georgia Institute of Technology**
Master's of *Computer Science* Specialised in Computing Systems (Online Programme)

Experience

September 2019 - Current | **Enflame Tech, Inc.** *Staff ASIC Design Engineer*
· Deep learning domain-specific accelerator architecture design and modeling
· Transaction model for architecture validation and verification
· Analytical model for architecture exploration and competitive studies
· Benchmarking on popular deep learning networks and frameworks
· Architecture performance validation and projection with transaction model.
· Intra-operator parallelism tuning with analytical and transaction model.
· DSL design and implementation for dataflow mapping of common operators.
· Analysis of compute, memory, and control flow characteristics of popular neural networks.

June 2017 - September 2019 | **NVIDIA, Inc.** *Senior GPU SM Architect*
· GPU SM (Streaming Multi-processor) behaviour modeling and test writing.
· Unit level behaviour modeling for Turing and Ampere.
· Convergence barrier instructions and friends.
· New instruction decoding and linting in function model.
· Fast SM modeling (with approximation) in fullchip simulator.
· Novel fast GEMM programming model with separate math and memory warps.
· Application tracing flow development, enhancement, and trace delivery.
· Performance verification and calibration with RTL implementation.
· Power planning, bridging, and competitive studies.
· Benchmarking on HPC, DL applications, and gaming graphics.

June 2016 - June 2017 | **Advanced Micro Devices, Inc.** *ASIC Layout/Design Engineer II*
· Develop and support for EDA / verification methodology tools:
· DSL for module-level connectivity and interface abstraction.
· User-guided design transformation:
· Module re-grouping for physical implementation.
· Low-power design generation using power-gating and clock-gating techniques.

February 2013 - April 2016 | **Synopsys, Inc.** *Intern, R&D Engineer I, R&D Engineer II*
· Software testing and test automation in *IC Compiler II*, focusing on
· *clock tree synthesis (CTS)* and *clock tree optimization (CTO)*
· *concurrent clock-data optimization (CCD)*
· CTS and CTO QoR tracking and optimization with low-power design.
· Internal tool developments:
· *a platform for test case indexing, searching, and analysis*
· *auto test creator based on patterns extracted from customer designs*
· *UPF generation with test hints*
· *data mining and feature extraction on test cases*

June 2012 - September 2012 | **Fudan Microelectronics, Inc.** *Intern*
· Error correction code (ECC) implementations on NAND flash study.

May 2011 - June 2013 | **ASIC State Key Laboratory, Fudan University** *Undergraduate Student*
· Focused on reconfigurable high performance computing on FPGA.
· *An extension of a light-weight OS running on FPGA*, offering abstraction and dynamic management of hardware reconfigurable computing resources for cryptographic applications. (undergraduate thesis, graded A);
· *Fault injection simulation* on lab-proprietary FPGA;
· Debugging tools for lab-proprietary FPGA: *QtViewer: an internal signal probe*, and *bitstream generation*.

Personal Projects

October 2018 | **Distributed System Design (CS6210 lab)**
· Implemented MapReduce infrastructure using google protobuf.

October 2018 | **Compiler Optimization for Embedded Computing Platform (CS6291 lab)**
· MIPS code generation optimization with instruction scheduling on VLIW, branch code optimization with data speculation.

October 2017 | **Lunar Lander Trained with Reinforcement Learning Algorithms (CS7642 lab)**
· Trained a lunar lander using DQN, double-DQN, and DDQN.

January 2017 | **Parallel / Distributed Algorithms Optimisation (CSE6220 lab)**
· Optimised parallel list-rank algorithm on multi-core machine.
· Optimised distributed terasort algorithm on multi-core machine using MPI.

April 2016 | CUDA MST
· Efficient minimum spanning tree CUDA implementation of data-parallel Boruvka's algorithm and data-parallel Kruskal's MST algorithm.

January 2016 | Cloud Computing Capstone
· Used Hadoop and Spark to analyse US flight data, on AWS EC2 clusters;
· Ranked airports and carriers by on-time-arrival performance, and searching for appropriate two-flight routes with specific temporal constraints.

September 2015 | Data Mining Capstone
· Analysed Yelp reviews, finished fundamental functionalities needed by a restaurant recommending system;
· Finished six tasks and one final report, covering topic mining, cuisine clustering and similarity analysis, dish recognition, restaurant recommendation, hygiene prediction.

November 2014 | Social Network Analysis on Github Repositories
· Final project of Coursera course Social Network Analysis, graded 98 / 100 by peers;
· Analysed the user-repository bipartite graph, its relationship with the community of language used by repositories, and its evolution over time.

Skills and Awards

Skills
Tcl, Python, C++/C, CUDA, Java, scala
ASIC physical design, timing analysis, CUDA programming, FPGA design, data mining

Certificates & Awards
· TOFEL 105; GRE Q170 V150 AWA 4.0;
· Data Mining Specialization and 14 Certificates of Accomplishment from Coursera;
· **Enflame** CEO Award, for initiating architecture performance evaluation framework (6 out of 300 employees);
· **NVIDIA** Top Contributor 2018, 2019 (top 5%);
· **AMD** Spotlight Award 2016, for outstanding deployment and support of a novel clock-gating methodology;
· **Synopsys** Best Mentor 2016, for excellent mentors of summer intern programmes;
· **Synopsys** Special Award for XTAGE 2016, for setting up an idea-sharing online forum;
· **Synopsys** STAR Award 2015, for top bug finders (2 out of 200 employees);
· **Fudan University** 2012, Scholarship for Excellent Students of Fudan University, Third Prize;
· **Fudan University** 2011, 2010, People's Scholarship of Fudan University, Third Prize;
· **Fudan University** 2011, Outstanding Student of Fudan University;
· **Fudan University** 2010, National Scholarship for Encouragement.